IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Patent Application No. 10/526,421

Confirmation No. 3287

Applicant: Leijten, Jeroen Anton Johan

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TC/AU: 2183

Examiner: Faherty, Corey S.

Docket No.: 260670 (Client Reference No. DJ/P82108US00)

Customer No.: 23460

APPELLANT'S APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In support of the appeal from the Final Office Action dated July 1, 2009, Appellant now submits his Brief.

Real Party In Interest

The patent application that is the subject of this appeal is assigned to Koninklijke Philips Electronics N.V.

Related Appeals and Interferences

There are no appeals or interferences that are directly related to this appeal.

Status of Claims

Claims 1-11, 13, and 15-17 are presently pending.

Claims 1-11, 13, and 15-17 stand rejected, and these rejections are presently being appealed.

Claims 12 and 14 are canceled.

Status of Amendments

There were no amendments submitted after the final rejection.

Summary of Claimed Subject Matter

Claims 1-11, 13, and 15-17 including independent claim 1 are pending. The summaries of the claims reference the specification and drawings filed with the application on March 1, 2005.

Independent **claim 1** pertains to a data processor comprising one or more functional units arranged to provide an internal processor pipeline, (see, Fig. 1, page 1, lines 23-27)

one or more register files, (see, Fig. 1, RF0/RF1, page 4, lines 2-4)

a data memory facility having a multibit access port facility, (see, Fig. 1, memory 40)

a snapshot buffer (Fig. 1, SS 20, shadow flipflops, page 4, lines 12-18), differing from the one or more register files (RF0/RF1), which during handling of an interrupt condition accommodates saving, by copying from the one or more register files to respective snapshot buffer elements, state information of various processor state elements, including state information from the internal processor pipeline, (see, page 5, lines 17-22) and

a controller means (SQ 26) arranged to save, upon occurrence of a subsequent interrupt condition during handling of an actual interrupt condition, the state information of various processor state elements currently within the respective snapshot buffer elements in the data memory facility having the multibit access port facility. (see, page 5, lines 23-30).

Grounds of Rejection to be reviewed on Appeal

The grounds of rejection to be reviewed on appeal are the grounds stated in the Office Action mailed on July 1, 2009. In particular, Appellant appeals:

1. The rejection of Claims 1-3, 5-7, 9, 13 and 15-17 under 35 U.S.C. §103(a) as obvious over Downing US Pat. No. 3,781,810 (Downing);

2. The rejection of Claim 4 under 35 U.S.C. §103(a) as being obvious over Downing in view of Petolino, Jr., et al. US Pat. No. 5,958,041 (Petolino);

3. The rejection of Claim 8 under 35 U.S.C. §103(a) as being obvious over Downing in view of Patterson et al., "Computer Organization & Design: The Hardware/Software Interface"(Patterson);

4. The rejection of Claim 10 under 35 U.S.C. §103(a) as being obvious over Downing in view of Forsyth US Pat. No. 5,327,566 (Forsyth); and

5. The rejection of Claim 11 under 35 U.S.C. §103(a) as being obvious over Downing in view of Lang et al., "Individual Flip-Flops with Gated Clocks for Low Power Datapaths"(Lang).

Argument

1. The Rejection of Claims 1-3, 5-7, 9, 13 and 15-17 as obvious over Downing

Appellant requests reversal of the Final Office Action's rejection of claims 1-3, 5-7, 9, 13, and 15-17 as obvious over Downing. A *prima facie* case of obviousness requires that the prior art reference(s) disclose, either expressly or inherently, each element of a rejected claim. Appellant seeks reversal of the Office Action's rejection of **independent claim 1** since Downing does not disclose at least one recited element of Appellant's claimed data processor.

Appellant's currently rejected claim 1 recites a "snapshot buffer" that saves state information during handling of an interrupt "including state information from the internal processor pipeline." Appellant submits that the teachings of Downing do not disclose the recited saving of "state information from the internal processor pipeline" within the snapshot buffer. Downing instead discloses *discarding internal pipeline state information in response to an interrupt*. Therefore the rejection of independent claim 1 should be reversed.

Appellant's Claimed Invention

Appellant's claim 1 recites a data processor including one or more functional units, one or more register files, a data memory, and a snapshot buffer. During handling of an interrupt condition, the snapshot buffer accommodates saving state information of various processor state elements, including *state information from the internal processor pipeline* provided by one or more functional units. The claimed data processor includes "controller means" (*see*, controller 26) that, upon entry of an interrupt processing state, saves state information of processor state elements (registers) currently within the snapshot buffer in the data memory facility having the multibit access port facility.

The claimed invention includes three distinct locations for saving state information of the data processor (i.e., register files, snapshot buffer, and data memory facility having a multibit access port facility). Initially, such information is stored within the register files of the processor. During interrupts, the processor saves state information from the register files to a snapshot buffer. Thus, the snapshot buffer differs from the recited register files and is provided *in addition*

to the one or more register files. Moreover, claim 1 specifically recites that the state information saved to the snapshot buffer includes *state information from the internal processor pipeline.* Furthermore, upon issuance of a subsequent interrupt, during processing of the subsequent interrupt, the contents of the snapshot buffer elements are transferred to the "data memory facility having the multiport facility" (making room in the snapshot buffer for saving state information from the internal processor pipeline).

Downing's Disclosed Computer

Downing discloses a program controlled computer which comprises independent control circuitry for exchanging data between registers R1, ..., Rn of the computer and the computer memory independently of the program execution. Downing's disclosed register/computer memory arrangement saves computer time as it facilitates the storing and retrieving of data which must be saved during nesting and unnesting of program transfers.

Downing discloses, for each register R1,...Rn that contains data which is to be saved upon the occurrence of a program interrupt, there is provided an auxiliary register AR1,...ARn and program controlled gates for exchanging data between each computer register and corresponding auxiliary register. However, as explicitly stated in column 3, lines 5-16, Downing's save operation is limited to *data* contained in registers R1..., Rn.

Non-Obvious Differences Between Downing and Appellant's Claimed Invention

The recited invention in claim 1 is not rendered obvious by Downing's disclosure since Downing discloses only storing *data* from a processor pipeline. Downing neither discloses nor suggests at least the recited element of a snapshot buffer that saves *state information from the internal processor pipeline.*

The Final Office Action, in section 7 (see, page 3, lines 9-12), concedes that Downing does not explicitly disclose that the system is pipelined. The Final Office Action states that the use and benefits of pipelining are notoriously well known in the art. The Final Office Action concludes that the techniques described by Downing, when applied to a well known pipelined processor structure, rendered the claimed saving of "state information from the internal processor pipeline" to a snapshot buffer obvious to one skilled in the art at the time of the invention.

However, this analysis is based upon Downing's disclosure of saving *data*, and the final rejection of claim 1 does not consider the actual recited element of "state information from the internal processor pipeline."

Appellant readily admits that pipelined processing and its benefits were known at the time of the invention. In fact, from FIGs. 1, 2A, and 2B of Downing it can be seen that the processor comprises pipelined elements. From FIG. 2B, it can be seen, in particular, that the Downing processor contains various *internal state elements*, including:

SAVR (element 32);
RESR (element 33);
ADDRESS REGISTER (element 16);
POINTER STORE (element 29);
BASE ADDRESS STORE (element 30); and
REGISTER ADDRESS STORE (element 44).

Despite the fact that Downing's processor (FIG. 1) has the above-identified state elements (FIG. 2b), only the *data* registers R1, ..., Rn have respective auxiliary registers AR1, ..., ARn that serve to temporarily save the *data* from the corresponding data registers. No such auxiliary storage is shown for the internal state elements depicted in FIG. 2b. Hence, while Downing explicitly shows an arrangement comprising a processor with data storage elements as well as internal state elements, and explicitly shows auxiliary registers for saving data from the data registers R1, ...,Rn, Downing does not disclose or suggest that *state information* from the internal pipeline is saved.

In support of Appellant's assertion that Downing does not disclose saving *state information* from the internal pipeline, Appellant notes that Downing indeed discloses pipelining in the processor component arrangement shown in Figure 2B. In particular, the elements "base address store 30" and "pointer store 29" form a pipeline with the address register 27. Also, before a next subroutine can be carried out, the above-identified pipeline must be flushed. Otherwise, the state information from the previous subroutine present in the elements 29, 30 would enter the element 27 when immediately executing the subsequent subroutine.

In accordance with the invention recited in claim 1, *the state information of the internal processor pipeline is saved to a snapshot buffer*. Such saving of a pipeline's internal state information enables a context switch in a single clock cycle (as opposed to multiple cycles needed when the internal processor pipeline state information is flushed).

Appellant submits that saving state information from the internal processor pipeline is not obvious in view of Downing since Downing discloses the presence of such state information (see above), yet Downing does not disclose saving this information during interrupts.

Appellant does not separately argue the patentability of Claims 2, 3, 5-7, 9, 13 and 15-17, but notes that each is dependent from claim 1, and therefore Appellant respectfully submits that these claims are not rendered obvious by Downing for at least the reasons set forth above regarding the final rejection of claim 1.

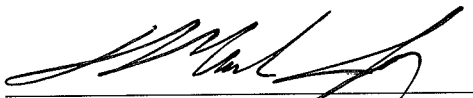
2-5. The rejections of Claims 4, 8, 10 and 11 as being obvious over Downing in view of Petolino, Patterson, Forsyth and Lang

To reduce the issues on appeal, Appellant will not separately argue the patentability of the dependent claims identified under the second through fifth grounds for rejection. However, Appellant reserves the right to argue the patentability of such claims at a later time if necessary.

Conclusion

In summary, the presently claimed invention is not rendered obvious by the teachings of the cited references since they do not disclose each element of the properly construed claims. The pending claims are patentable over the prior art presently known to Appellant. Appellant therefore requests reversal of the rejection of claims 1-11, 13 and 15-17.

Respectfully submitted,



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Claims Appendix

1. (Previously presented) A data processor comprising:

one or more functional units arranged to provide an internal processor pipeline,

one or more register files,

a data memory facility having a multibit access port facility,

a snapshot buffer, differing from the one or more register files, which during handling of an interrupt condition accommodates saving, by copying from the one or more register files to respective snapshot buffer elements, state information of various processor state elements, including state information from the internal processor pipeline, and

a controller means arranged to save, upon occurrence of a subsequent interrupt condition during handling of an actual interrupt condition, the state information of various processor state elements currently within the respective snapshot buffer elements in the data memory facility having the multibit access port facility.

2. (Previously Presented) The data processor as claimed in Claim 1, wherein said controller means are arranged to retrieve the saved contents of said snapshot buffer elements from said data memory facility through said multibit access port facility back into said snapshot buffer elements upon completing the handling of the actual interrupt condition.

3. (Previously Presented) The data processor as claimed in Claim 2, wherein said controller means are arranged to restore the retrieved saved state information of various processor state elements allowing said data processor to proceed with handling one of an earlier uncompleted interrupt or continuing a main thread of the processing.

4. (Previously Presented) The data processor as claimed in Claim 1, wherein said state information comprise latency data of current operations.

5. (Previously Presented) The data processor as claimed in Claim 1, wherein said snapshot buffer comprises output multiplexer means having said multibit access port facility for

sequentially saving selected snapshot buffer elements for transferring to said data memory facility.

6. (Previously Presented) The data processor as claimed in Claim 1, wherein said snapshot buffer comprises input multiplexer means having said multibit access port facility for sequentially selecting selected snapshot buffer elements for back-transferring from said data memory facility.

7. (Previously Presented) The data processor as claimed in Claim 1, wherein said data memory facility is operated as a stack.

8. (Previously Presented) The data processor as claimed in Claim 7, wherein said stack has a stack pointer that allows multiple stack positions per snapshot.

9. (Previously Presented) The data processor as claimed in Claim 7, wherein said snapshot buffer comprises input multiplexer means having said multibit access port facility for sequentially selecting selected snapshot buffer elements for back-transferring from said data memory facility, wherein said snapshot buffer comprises output multiplexer means having said multibit access port facility for sequentially saving selected snapshot buffer elements for transferring to said data memory facility, and wherein write and read operations in said stack are executed at mutually exclusive instants in time under control of a stack pointer.

10. (Previously Presented) The data processor as claimed in Claim 1, wherein said snapshot buffer is at least substantially constructed from shadow flipflops for storing its snapshot information.

11. (Previously presented) The data processor as claimed in Claim 1, wherein said snapshot buffer is operated at low power through one or more of clocking shadow flipflops only during actual taking of a snapshot, clocking only the shadow flipflops pointed to by a stack pointer as a top-of-stack-plus-one during a stack push operation, and clocking the stack pointer itself only during stack pointer updates that are caused by popping and pushing of a snapshot buffer stack.

12. (Canceled)

13. (Previously Presented) A data processing facility comprising the data processor as claimed in claim 1.

14. (Canceled)

15. (Previously Presented) The data processing facility as claimed in Claim 1, wherein the controller means is arranged to save the various processor state elements to the respective snapshot buffer elements in a single clock cycle.

16. (Previously Presented) The data processing facility as claimed in Claim 1, wherein the controller means is arranged to restore the various processor state elements from the respective snapshot buffer elements in a single clock cycle.

17. (Previously presented) The data processing facility of Claim 1, wherein the controller means saves, upon occurrence of the subsequent interrupt condition during the handling of an actual interrupt condition, the state information of various processor state elements currently within the respective snapshot buffer elements in the data memory facility using a stack pointer, an wherein no additional instruction bits are required for addressing the snapshot buffer elements.

Evidence Appendix

NOT APPLICABLE

Related Proceedings Appendix

See "Related Appeals and Interferences" section above.